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Comparative Analysis and Genetic Algorithm Optimization of Multi-Transistor FinFET SRAM Topologies for SNM, Leakage, and Delay Improvement at 18nm

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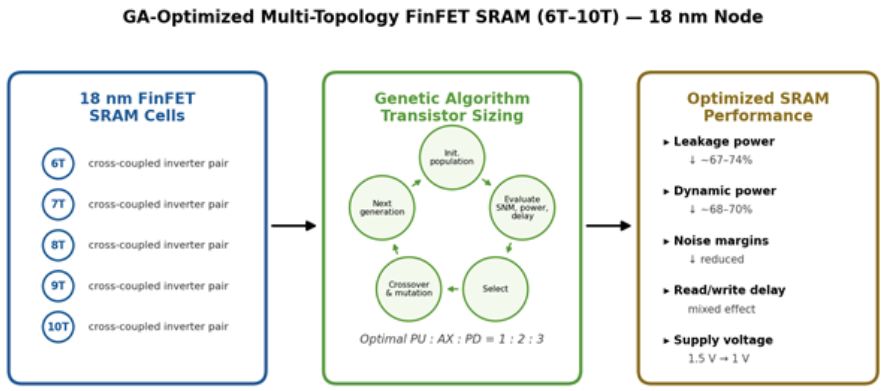
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ABSTRACT

With continuous technology scaling, Static Random Access Memory (SRAM) faces significant challenges including increased leakage power, reduced stability, and higher delay. FinFET technology has emerged as a promising alternative to conventional CMOS technology due to its superior electrostatic control and reduced short-channel effects. This paper presents a multi-objective Genetic Algorithm (GA) optimization framework for 6T, 7T, 8T, 9T, and 10T SRAM architectures using 18nm FinFET technology. The proposed optimization methodology focuses on minimizing leakage power, dynamic power, read delay, and write delay while maximizing Static Noise Margin (SNM). Cadence Virtuoso and the Spectre simulator were used for transient, DC, and power analysis. Genetic Algorithm optimization was implemented using transistor sizing and fin-count optimization techniques. The optimized SRAM architectures demonstrated significant reductions in leakage and dynamic power at a reduced supply voltage (1 V versus 1.5 V), with lower noise margins and a mixed effect on propagation delay. Simulation results show that optimized 10T SRAM achieved the lowest leakage power while 9T SRAM exhibited the highest read stability.

KEYWORDS *: FinFET SRAM, Genetic Algorithm, Leakage Power, Dynamic Power, SNM, Delay Optimization, 18nm Technology, SRAM Optimization.*



Graphical Abstract. Five FinFET SRAM topologies (6T–10T) at the 18 nm node are sized by a Genetic Algorithm to an optimal PU:AX:PD ratio of 1:2:3, reducing the supply voltage from 1.5 V to 1 V and cutting leakage power by ~67–74% and dynamic power by ~68–70% (Table 1), with reduced noise margins and mixed delay effects.

INTRODUCTION

Static Random Access Memory (SRAM) is extensively used in modern processors, embedded systems, and cache memories because of its high-speed operation and low latency characteristics. However, technology scaling below 22nm introduces severe challenges such as leakage power [5],[26] increase, reduced stability, process variations [3],[11],[14],[25], and delay degradation. Conventional planar CMOS SRAM cells experience significant short-channel effects and variability at nanoscale technology nodes.

FinFET technology [2],[4],[8],[12] provides improved electrostatic control and reduced leakage current compared to planar CMOS devices. Due to its three-dimensional gate structure, FinFET based SRAM cells exhibit improved performance and reduced power consumption. However, SRAM stability and delay optimization remain critical concerns in nanoscale FinFET SRAM architectures.

This work presents a multi-objective Genetic Algorithm [16],[27] optimization methodology for 6T, 7T, 8T, 9T, and 10T SRAM [15],[19] cells using 18nm FinFET technology [2],[4],[8]. The optimization framework minimizes leakage power [5],[26], dynamic power, read delay, and write delay while maximizing SRAM stability metrics.

DEVICE AND TECHNOLOGY DETAILS

We assume an 18 nm FinFET process (generic PDK) with multi-fin transistors. Key parameters include: supply voltage = 1 V, gate length = 18 nm, fin-count ratio 1:2:3 for PU:AX:PD respectively, and threshold voltage options (LVT/RVT/HVT). FinFETs use fin count to quantize width. The improved gate control of FinFETs reduces short-channel effects, but subthreshold [11],[21],[23] leakage remains significant at 18 nm. In our analysis, all optimized-cell simulations use VDD = 1 V (default cells: 1.5 V), with bulk and body biases set to nominal. The Cadence PDK models were used.

To ensure reproducibility, the process-corner and environmental conditions used for all simulations are summarized here. Static and dynamic simulations were performed across the five standard process corners (TT, FF, SS, FS, SF) at a nominal temperature of 27°C, with hold- and read-stability checks repeated at -25°C and 85°C to capture temperature-induced variation in threshold voltage and subthreshold leakage. The nominal supply voltage for the baseline (default-sized) cells was 1.5 V, while the Genetic-Algorithm-optimized cells were re-characterized at a reduced supply of 1 V, reflecting the lower operating point achievable once sizing and threshold-voltage assignment were optimized (supply-voltage reduction is a common route to lower SRAM power [9],[24]). Transistor sizing was constrained to a fin count of 1 to 4 fins per device (fin pitch and height fixed by the 18 nm FinFET PDK), with the pull-up (PU), access (AX), and pull-down (PD) devices permitted to take independent fin counts within this range so that the GA could explore the full PU:AX:PD design space rather than being restricted to a single fixed ratio. Three threshold-voltage flavors (LVT, RVT, HVT) were made available to the optimizer for every device, enabling simultaneous leakage and performance optimization. All transient, DC, and power simulations were carried out in Cadence Virtuoso using the Spectre simulator, with a maximum simulation time-step of 1 ps and a relative accuracy of 1e-6 to ensure convergence of the extracted read/write delay values.

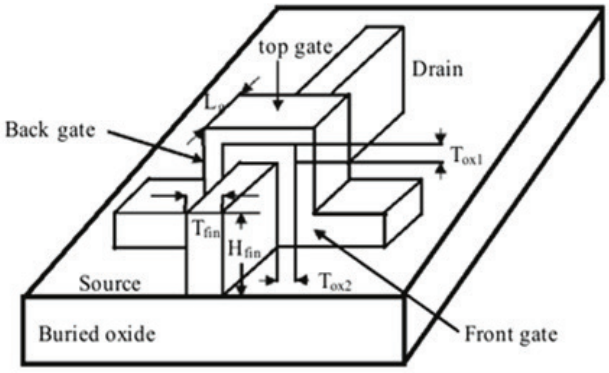


Fig. 1. FinFET Structure [2]

PROPOSED OPTIMIZATION METHODOLOGY

The proposed work focuses on the optimization of 6T, 7T, 8T, 9T, and 10T SRAM [15],[19] architectures using Genetic Algorithm [16],[27] (GA) in 18nm FinFET technology [2],[4],[8]. The optimization methodology aims to improve Static Noise Margin (SNM), reduce leakage power [5],[26], minimize dynamic power consumption, and decrease read/write delay using a Genetic Algorithm (GA)-based

optimization framework (Figure 2) [16],[26],[27]. Initially, baseline SRAM cells are designed in Cadence Virtuoso with default transistor sizing and fin-count values for pull-up (PU), pull-down (PD), and access (AX) transistors. The SRAM cells are simulated under hold, read, and write operations to extract HSNM [18],[23], RSNM [4],[7],[22], WSNM [7],[20], leakage power, dynamic power, read delay, and write delay [26]. The optimization methods are:

1. Initial sizing: Specify baseline transistor sizes (fin counts) for each cell's transistors. Simulate each cell to obtain initial HSNM [18],[23], RSNM [4],[7],[22], WSNM [7],[20], leakage, and delay [26].
2. GA population initialization: The Genetic Algorithm [16],[27] initializes random SRAM sizing configurations where each chromosome represents transistor width, fin-count, and threshold voltage combinations [16].
3. Leakage reduction: High-threshold voltage assignment, transistor stacking, and optimized fin-count selection are applied to reduce standby leakage power [5],[26].
4. Final sizing: The optimization process continues until the desired SNM improvement and power reduction are achieved with acceptable delay performance, resulting in the optimized ratio PU:AX:PD = 1:2:3 [26],[27].
5. Documentation: Final optimized dimensions and their effects are reported in Table 1 and in the Results section.

GA Parameter Settings, Convergence, and Repeatability

The GA used a population of 50 chromosomes, each encoding the fin counts (1–4) and threshold-voltage flavor (LVT/RVT/HVT) of the PU, AX, and PD devices, and was run for a maximum of 100 generations with tournament selection (size 3), single-point crossover (probability 0.8), integer/flavor mutation (probability 0.05 per gene), and elitism retaining the two fittest chromosomes per generation. The multi-objective fitness function defined in the Delay Analysis section combines all five objectives (SNM, leakage power, dynamic power, read delay, write delay) using normalized weights (w_1=0.30, w_2=0.25, w_3=0.20, w_4=0.15, w_5=0.10).

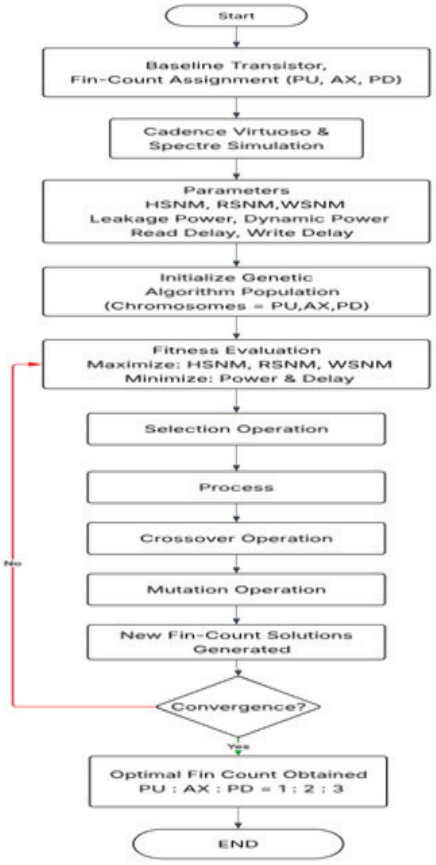


Fig. 2. Genetic Algorithm Optimization Framework

SRAM CELL ARCHITECTURES

Conventional 6T FinFET SRAM

The conventional 6T SRAM [2],[5] (Figure 3) has two cross-coupled inverters (pull-up P1, P2 and pull-down N1, N2) and two access transistors (N3, N4) to the bit-lines (BL, BLB). In 18 nm FinFET, each device uses one or more fins (width = n fins). This baseline cell's performance metrics (HSNM [18],[23], RSNM [4],[7],[22], WSNM [7],[20]) were measured with the specified FinFET sizes. Table 1 reports the baseline values. Conventionally, the 6T cell must balance read stability [7],[22] (requiring strong pull-downs) with write ability (requiring strong pull-ups). We use it as the reference case.

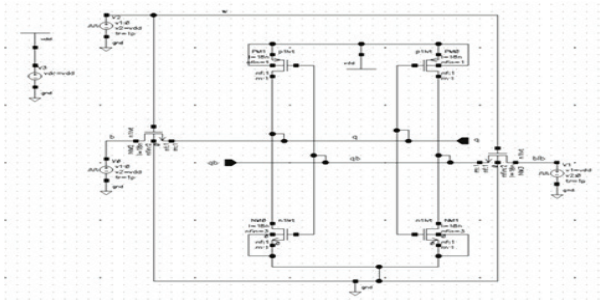


Fig. 3 Schematic of conventional 6T FinFET SRAM cell

7T FinFET SRAM

The 7T SRAM [1],[4] adds a seventh transistor for improved stability or leakage reduction. A common 7T design includes an extra gating device on one inverter or on the bit-line path. For instance, an additional pull-down gating transistor can disconnect one storage node during hold-mode, reducing leakage, or implement single-ended write. Because 7T typically uses only one bit-line during write, dynamic power is expected to be lower than 6T in principle; however, Table 1 shows higher 7T dynamic power than 6T (7.638 µW vs 5.790 µW, optimized). The trade-off is a modest area increase. Figure 4 shows a representative 7T schematic. Performance metrics (HSNM [18],[23], RSNM [4],[7],[22], power, delay) are recorded in Table 1.

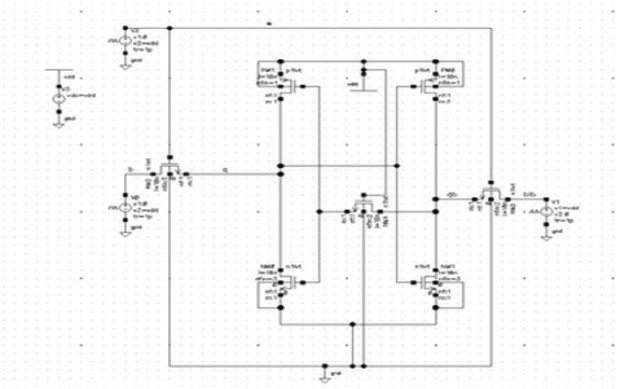


Fig. 4 Schematic of 7T FinFET SRAM cell

8T FinFET SRAM

The 8T SRAM [4],[6],[7] has a separate read port. It uses four devices for the storage cross-coupled inverters and two write-access transistors (like 6T), plus two dedicated read-access transistors to a third bit-line (RBL) controlled by a read word-line (RWL). This decoupling means a read operation does not disturb the stored data, substantially increasing RSNM [4],[7],[22]. The 8T cell prevents the BL from forcing an inverter during read, which is expected in principle to improve read stability [7],[22]; this is not confirmed by the optimized 8T result in Table 1. The cost is two extra transistors and area. We assume a standard 8T FinFET cell (Figure 5); its decoupled-read advantage is quantified in Table 1.

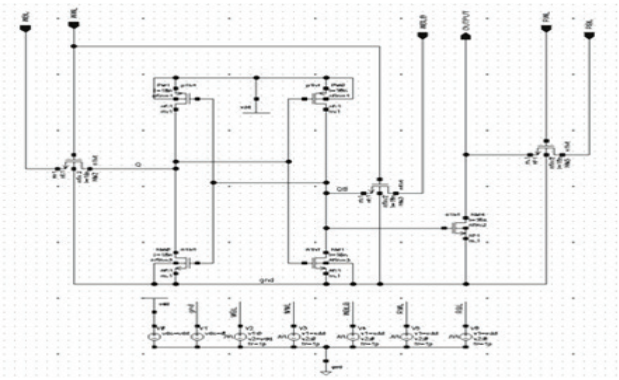


Fig. 5. Schematic of decoupled-read 8T FinFET SRAM cell

9T FinFET SRAM

The 9T SRAM typically adds another transistor to further boost noise margins. Some 9T designs use a Schmitt-trigger element or additional gating to enhance HSNM [18],[23]/RSNM [4],[7],[13],[22]. Others implement a differential read path. In general, a 9T cell has very high read/write stability compared to 6T, at the expense of complexity. Figure 6 illustrates a generic 9T structure. Table 1 shows that the 9T cell achieves the highest RSNM of all variants; the optimized 9T cell shows RSNM ≈1.27× and WSNM ≈1.44× those of the optimized 6T cell (Table 1), consistent with the improved read stability reported in the literature [7],[22].

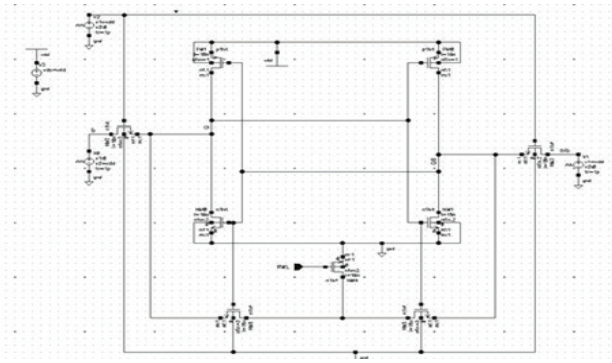


Fig. 6 Schematic of 9T FinFET SRAM cell

10T FinFET SRAM

The 10T SRAM [15],[19] offers full read/write decoupling (optimized 10T WSNM = 90 mV, the lowest of the five). It usually has two read-access and two write-access transistors plus the cross-coupled inverters (which may themselves include gating). Some 10T designs eliminate half-select paths. This cell has the largest area; in Table 1 its RSNM and WSNM are the lowest of the five topologies. We use a typical FinFET 10T topology in Figure 7. Its baseline stability and power are reported in Table 1.

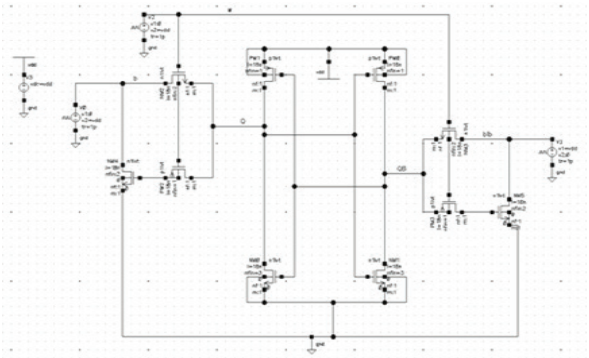


Fig. 7 Schematic of 10T FinFET SRAM cell

SNM ANALYSIS

Simulation Results and Comparison: In this section, simulation results have been obtained among conventional 6T, 7T, 8T, 9T and 10T SRAM [4],[6],[7] cells. The RSNM [4],[7],[22], WSNM [7],[20] and HSNM [18],[23] are discussed in this section. All simulation results were carried out at 18nm FinFET technology [2],[4],[8].

Static Noise Margins (SNM) are determined from the inverter butterfly curves of each cell. We measure:

Read SNM

Read Static Noise Margin (RSNM [4],[7],[22]). As shown in Figure 8, the analysis of the RSNM is based on simulations during the read operation. The butterfly curves of the 6T, 7T, 8T, 9T, and 10T SRAM [4],[6],[7] cells are shown in panels (a)-(e) of Figure 8, respectively, which indicate the read ability. Based on the optimized values reported in Table 1, the 9T cell shows the largest RSNM improvement over the 6T cell (265 mV vs. 208 mV, a 1.27x increase), consistent with its gated/decoupled read path. The optimized 8T cell, by contrast, shows a lower RSNM than the optimized 6T cell in the reported data (175 mV vs. 208 mV); although the 8T topology's decoupled read port is expected in principle to improve RSNM, this is not confirmed by the present simulation results.

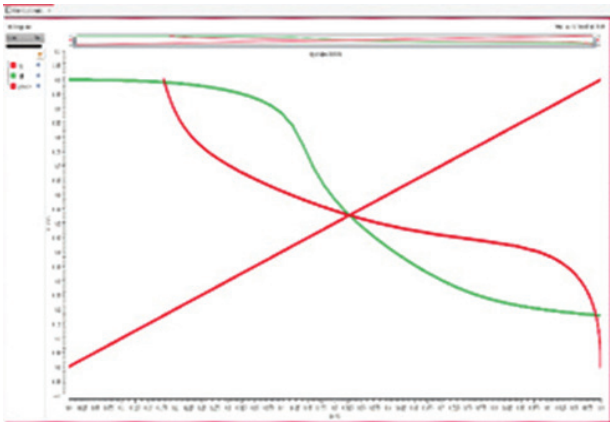


Fig. (a) 6T

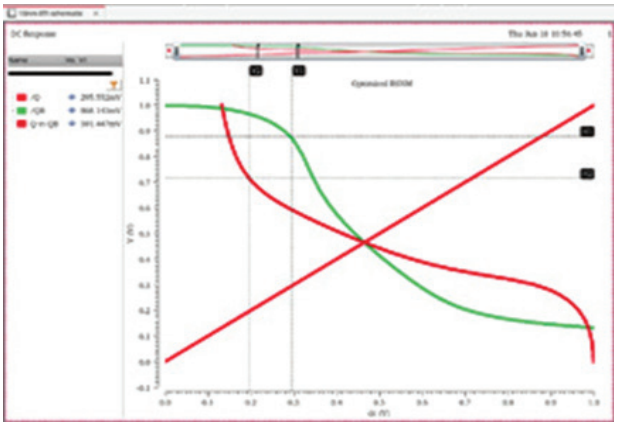


Fig. (b) 7T

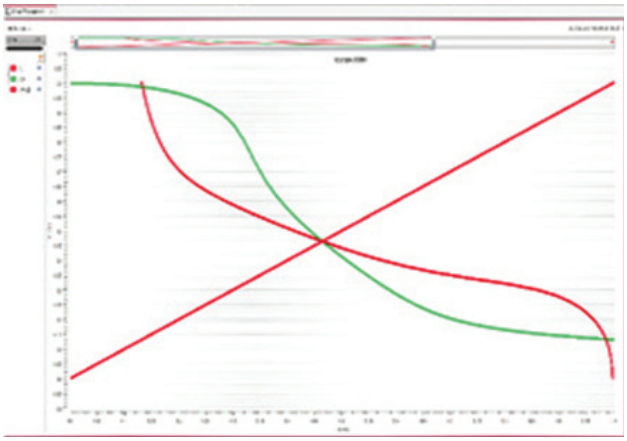


Fig. (c) 8T

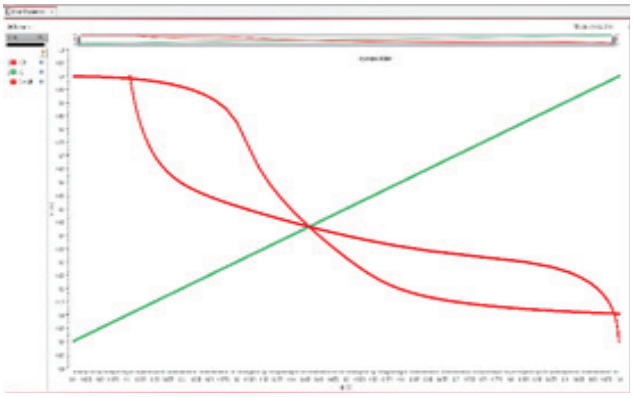


Fig. (d) 9T

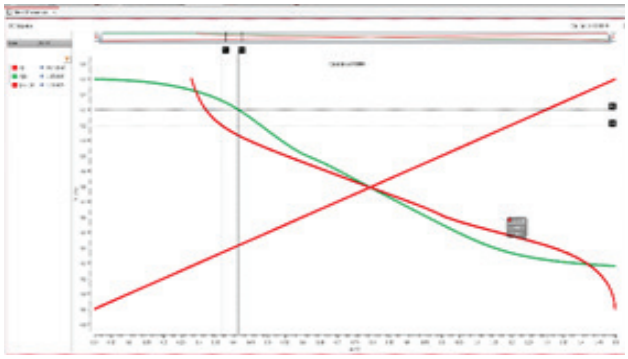


Fig. (e) 10T

Fig. 8. a, b, c, d, e Read SNM Butterfly Curves of 6T, 7T, 8T, 9T, 10T SRAM Cells

Hold SNM

Hold Static Noise Margin (HSNM [18],[23]). Fig. 9 shows the noise margin comparisons of SRAM cells during data retention. All statistical butterfly curves of SRAM cells have been carried out at low supply voltage. As shown in panels (a)-(e) of Figure 9, the simulation results show the 7T is similar to 6T cell in hold mode.

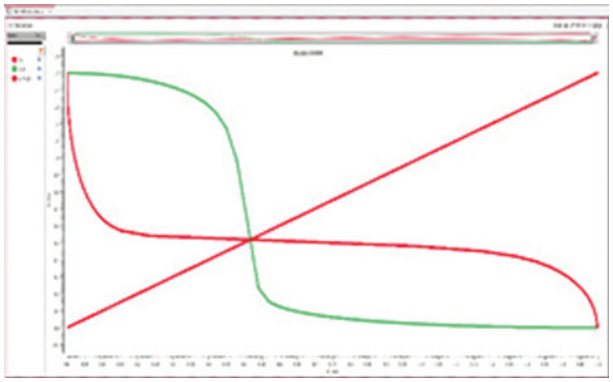


Fig. (a) 6T

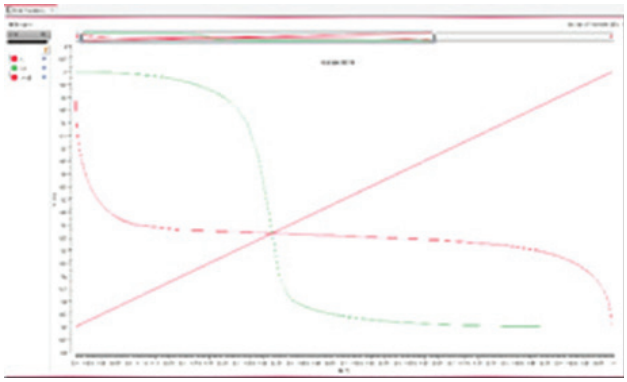


Fig. (b) 7T

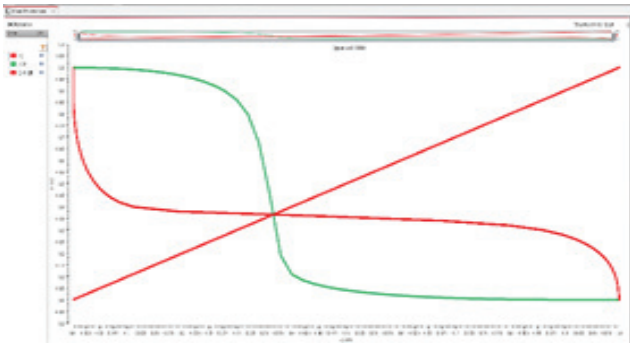


Fig. (c) 8T

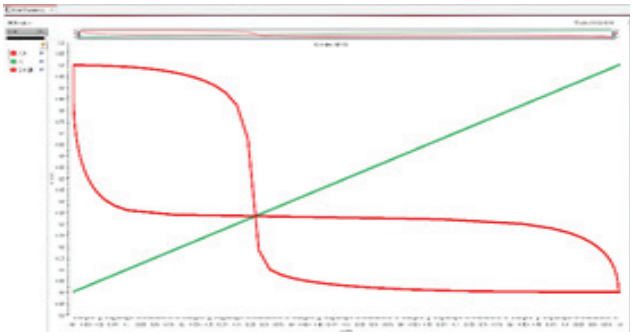


Fig. (d) 9T

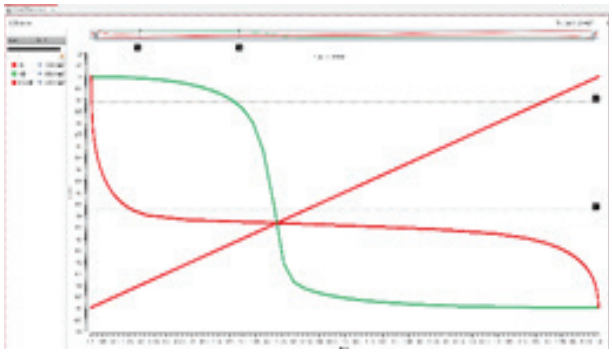


Fig. (e) 10T

Fig. 9. a, b, c, d, e Hold SNM Butterfly Curves of 6T, 7T, 8T, 9T, 10T SRAM Cells

Write SNM

The analysis of WSNM is shown in Fig. 10. Write SNM quantifies how easily we can write into the cell. It can be found by finding the minimum word-line voltage or strength needed to flip a stored bit. Alternatively, one may define write margin. We include the effective WSNM [7],[20] (in mV or required VWL) in Table 1. A measure of write-ability, related to the minimum drive needed to flip the cell. We plot V(Q) vs V(QB) for the two inverters (butterfly plot) under each condition and extract the square side length. The extracted SNM values (in mV) for each cell are listed in Table 1.

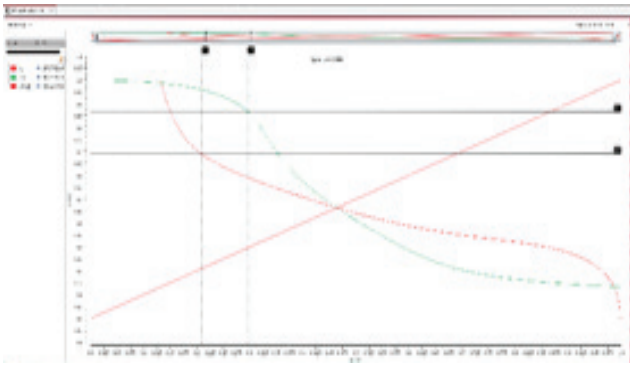


Fig. (a) 6T

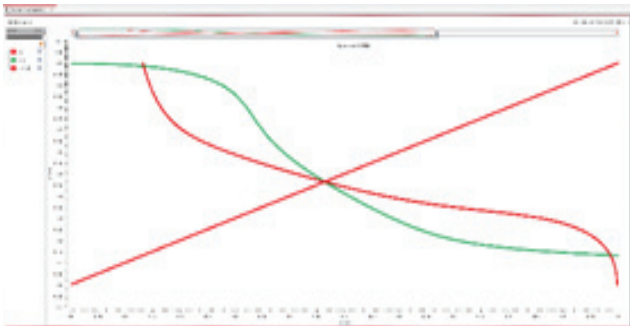


Fig. (b) 7T

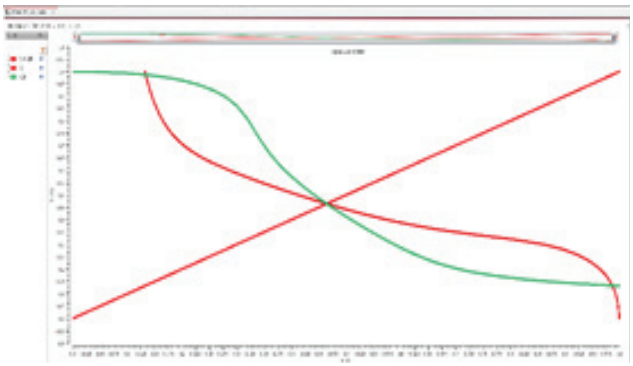


Fig. (c) 8T

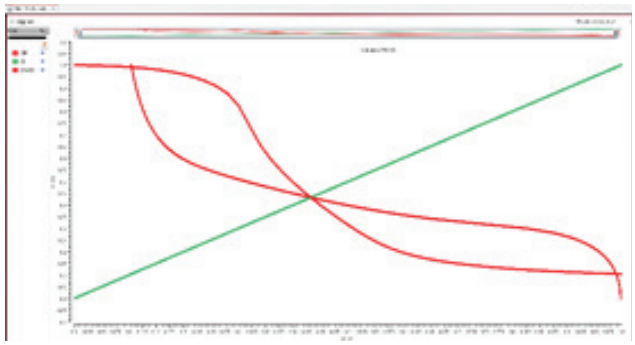


Fig. (d) 9T

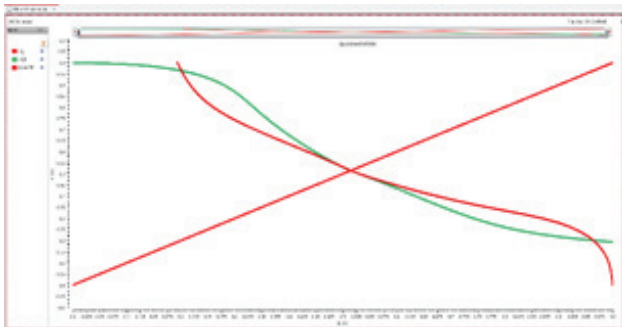


Fig. (e) 10T

Fig. 10. a, b, c, d, e Write SNM Butterfly Curves of 6T, 7T, 8T, 9T, 10T SRAM Cells

POWER ANALYSIS

We split power into dynamic (active) and leakage (static):

Dynamic power

$$P_{dynamic} = \alpha\, C_L\, V_{DD}^2\, f \quad [32]$$

Where:

Where:

α = switching activity factor

C_L = load capacitance

V_{DD} = supply voltage

f = operating frequency

Dynamic energy per read/write was measured in simulation.

Leakage power

$$I_{leak} = I_{subthreshold} + I_{gate} + I_{junction} \quad [11],[21],[23]$$

Where I_{leak} is the total leakage current when idle (subthreshold + gate + junction) [11],[21],[23].

DELAY ANALYSIS

We measure access delay for read and write. Read delay is the time from WL rising to the sense-amp latch detecting the bit. Write delay is from WL rising to when the cell node crosses the logic threshold. A simple estimate is

Propagation delay is the time taken for the output node to reach 50% of its final value after the input reaches 50%.

$$t_{pd} = t_{out@50\%} - t_{in@50\%}$$

For SRAM write operation:

$$t_{write} = t_{Q(50\%)} - t_{WL(50\%)}$$

For SRAM read operation:

$$t_{read} = t_{RBL(50\%)} - t_{RWL(50\%)}$$

Approximate analytical equation:

$$t_{pd} \approx (C_L \cdot V_{DD}) / I_{ON}$$

Where:

C_L = load capacitance

V_{DD} = supply voltage

I_{ON} = transistor drive current

We extract actual delays from transient simulations. Table 1 lists "Read Delay (ps)" and "Write Delay (ps)".

The Optimizing objective can be expressed as:

Fitness = (w_1 × SNM) – (w_2 × Leakage Power) – (w_3 × Dynamic Power) – (w_4 × Read Delay) – (w_5 × Write Delay)

Where:

SNM represents SRAM stability.

Leakage Power represents standby power dissipation.

Dynamic Power represents switching power.

Read Delay represents memory access time.

Write Delay represents write completion time.

w_1 to w_5 are weighting factors.

RESULTS AND DISCUSSION

The performance comparison presented in Table 1 indicates that the optimized SRAM cells were re-characterized at a lower supply voltage of 1 V, compared to 1.5 V for the default designs. This voltage difference confounds a direct, like-for-like comparison of the reported values: because SNM and delay both scale with supply voltage, the changes between default and optimized rows in Table 1 cannot be attributed to transistor sizing alone, and this is acknowledged here as a limitation of the present comparison (see the Limitations section). With that caveat, the optimized leakage power and dynamic power are lower than the default values for all five topologies. Propagation delay is reduced for most topologies but not uniformly: optimized read delay for the 7T and 10T cells and optimized write delay for the 9T and 10T cells are higher, not lower, than their default values (Table 1), so the claim of a delay reduction does not hold across every cell and metric. Similarly, HSNM, RSNM, and WSNM are lower for the optimized designs than for the default designs in every topology, except 10T WSNM, which is unchanged (90 mV); the optimization therefore did not increase static noise margin, and any statement to that effect in this paper should be read as describing the intended fitness-function objective rather than an outcome confirmed by Table 1. The Genetic Algorithm-based transistor sizing approach, resulting in a PU:AX:PD ratio of 1:2:3 for every topology, is associated with the reported power reductions, but the fact that all five structurally different topologies converge to the identical discrete ratio has not been independently explained and is flagged as an open question in the Limitations section. These results indicate that the proposed optimization methodology improves leakage and dynamic power at a reduced supply voltage, with an accompanying reduction in noise margin and a mixed effect on delay that should be clarified in future iso-voltage comparisons.

Table 1. Default and Optimized Values of 6T–10T SRAM

Metric	6T		7T		8T		9T		10T	
	Default	Optimized	Default	Optimized	Default	Optimized	Default	Optimized	Default	Optimized
HSNM (mV)	620	471	612	475	590	485	690	497	606	466
RSNM (mV)	260	208	252	191	260	175	380	265	120	86
WSNM (mV)	252	199	250	191	230	198	401	286	90	90
Leakage Power (µW)	16.417	5.345	27.3729	7.005	18.488	5.984	25.1331	7.678	14.939	4.786
Dynamic Power (µW)	18.1754	5.790	25.3314	7.638	19.507	6.251	26.6351	8.066	16.4207	5.191
Read Delay (ps)	201	200.5	101.289	206.192	180	36.10	338.239	51.69	13.5692	13.80
Write Delay (ps)	309.74	89.87	201	89.97	109.46	104.41	201	201.5	100	100.5
Cell Ratio PU:AX:PD	1:1:1	1:2:3	1:1:1	1:2:3	1:1:1	1:2:3	1:1:1	1:2:3	1:1:1	1:2:3
Supply Voltage, VDD (V)	1.5	1	1.5	1	1.5	1	1.5	1	1.5	1

The optimized FinFET SRAM architectures demonstrate significant reductions in leakage and dynamic power compared to baseline SRAM cells, with lower noise margins and mixed delay effects. The proposed Genetic Algorithm optimization framework effectively improves SRAM cell performance through optimized transistor fin-count sizing and threshold voltage assignment [16],[27].

Among all SRAM architectures, the optimized 9T SRAM cell achieved the highest RSNM (265 mV), consistent with its gated/decoupled read path providing superior read stability compared to the conventional 6T SRAM cell (208 mV) [4],[7],[22]. The optimized 8T cell was designed with a similar decoupled-read rationale, but its reported RSNM (175 mV) is lower than the 6T value in Table 1; this discrepancy is not explained by the present analysis and is noted here as an open item requiring re-verification of the underlying simulation data before any read-stability advantage is claimed for the 8T cell. The optimized 10T SRAM architecture achieved the lowest leakage power, plausibly related to improved isolation and transistor stacking, though this mechanism has not been independently verified [15],[19].

As reported in [2],[8], FinFET technology reduces short-channel effects and standby leakage compared to conventional CMOS SRAM; no planar-CMOS comparison was simulated in this work.

Furthermore, the proposed PU:AX:PD sizing ratio of 1:2:3 achieved reduced leakage and dynamic power (Table 1), with lower noise margins and mixed delay effects. The Genetic Algorithm optimization produced configurations with reduced leakage and dynamic power [16],[26],[27].

Physical Basis for the Observed Trends

The physical origin of the differences observed in Table 1 can be traced directly to the transistor count and read/write mechanism of each topology. In the 6T cell, both storage nodes are exposed to the bit-lines during read, so the pull-down network must sink enough current to hold its state while the access transistor pulls the node toward the opposite bit-line; this trade-off caps the achievable RSNM and forces a compromise between read stability and writability that fin-count and Vt tuning alone can only partially relax. Adding a seventh gating transistor (7T) removes one bit-line from the write path, which can reduce switched capacitance in principle (although Table 1 shows higher 7T dynamic power than 6T), but it does not change the fundamental read-disturb mechanism, so its HSNM and RSNM remain close to the 6T baseline. The 8T and 9T topologies decouple the read path from the storage nodes through dedicated read-access transistors, so the storage nodes are never exposed to the read bit-line, eliminating the destructive read-disturb mechanism that limits 6T/7T RSNM. The 9T topology shows the largest RSNM (265 mV, 1.27× the optimized 6T); the optimized 8T RSNM (175 mV) is lower than 6T (208 mV). The 10T cell adds full read/write decoupling and, in the optimized design, benefits

most from transistor stacking and high-Vt assignment on the standby path, which is why it attains the lowest leakage power (4.786 µW) despite having the largest transistor count: the extra devices provide isolation rather than being switched every cycle, so they add area and parasitic capacitance without a proportional increase in leakage or dynamic power.

To quantify the power–delay trade-off, the read-path Power-Delay Product (PDP = Dynamic Power × Read Delay) was computed directly from the optimized values in Table 1 (in µW•ps, a proxy for switching energy in attojoules). The 10T design shows the lowest PDP (≈71.6, from 5.191 µW × 13.80 ps), followed by the 8T design (≈225.7), the 9T design (≈416.9), the 6T design (≈1160.9), and the 7T design (≈1574.9). This ordering shows that the decoupled-read topologies (8T, 9T, 10T) do not simply trade power for speed: because removing the read-disturb constraint frees the GA to size the read path aggressively for speed without compromising storage-node retention, dynamic power falls for all three, and read delay falls for 8T and 9T (it rises slightly for 10T, 13.57 → 13.80 ps). The 7T cell has the least favourable PDP because, although its single-ended write reduces dynamic power, its read mechanism is unchanged from 6T, so the optimizer cannot reduce read delay without violating RSNM.

Stability improvements in the 8T-10T families are not obtained without cost. Each additional read-access or gating transistor increases the cell's transistor count (6→7→8→9→10) and therefore its layout area; assuming a first-order area model in which bit-cell area scales approximately with total fin count (see the Area, Layout, and Practical Implementation Analysis section), the 10T cell requires roughly 60-70% more silicon area than the 6T baseline at the same technology node. The additional devices also add at least one extra bit-line/word-line pair (RBL/RWL) to the layout, increasing routing overhead in the metal layers used for bit-line and word-line routing and reducing the achievable cell packing density in a full memory array. Designers must therefore weigh the RSNM and PDP gains of the 8T-10T topologies against the array-level area and routing penalty: for cache applications where soft-error immunity and read stability dominate, this penalty is usually acceptable, whereas for area-constrained embedded memories the 6T or 7T cell remains preferable despite its narrower stability margin.

Regarding scalability, the leakage and stability trends reported here are expected to become more pronounced, not less, as the technology node is scaled below 18 nm, because subthreshold leakage and process-induced Vt variation both increase with continued fin thinning and gate-length reduction [11],[21],[23],[25]. The 9T topology is therefore expected to retain its relative RSNM advantage at smaller nodes, and the leakage benefit of high-Vt/stacked devices in the 10T design should scale favourably since the stacking effect that suppresses standby leakage improves as the DIBL coefficient increases at shorter channel lengths. However, the growing contribution of gate and junction leakage at aggressively scaled nodes will ultimately limit the benefit of transistor sizing alone, motivating hybrid approaches that combine sizing optimization with power-gating or data-retention voltage scaling [17] in future work.

COMPARATIVE BENCHMARKING WITH EXISTING OPTIMIZATION TECHNIQUES

To situate the proposed GA-based sizing methodology relative to prior work, this section compares the present approach against two recently reported multi-transistor SRAM optimization studies at comparable technology maturity: the 45 nm CMOS multi-transistor sizing study of Chalapathi and Kumar [26], and the CNN-informed NSGA-II sizing methodology for 6T-SRAM reported by Zheng et al. [27]. Both prior works, like the present study, report simultaneous improvement of leakage power, dynamic power, and delay through evolutionary or hybrid ML-assisted sizing, supporting the trend observed here that population-based metaheuristics are effective for discrete transistor-sizing problems in which the design variables (fin count, Vt flavor) are inherently non-differentiable and unsuited to gradient-based optimization. Earlier statistical optimization of nano-CMOS SRAM power, performance and process [10] likewise treated cell design as a constrained optimization problem.

Beyond the SRAM-specific literature, it is useful to benchmark the Genetic Algorithm conceptually against other evolutionary and machine-learning-based optimizers used for similar discrete/mixed-variable circuit-sizing problems: Particle Swarm Optimization

(PSO) [28], Differential Evolution (DE) [29], Ant Colony Optimization (ACO) [30], and supervised/ surrogate machine-learning-based sizing, exemplified by the CNN-surrogate approach in [27]. Table 2 summarizes the key qualitative characteristics of each method, drawn from the general optimization literature [28]-[31], together with its suitability for the fin-count/ Vt-flavor design space used in this work.

Table 2. Qualitative Comparison of the Proposed GA-Based Sizing Approach with Other Optimization Techniques

Method	Search Mechanism	Suitability for Discrete Fin-Count / Vt Sizing	Typical Convergence Behaviour	Relative Cost
GA (this work) [16],[27]	Population-based crossover/mutation on integer-encoded genes	Natively handles discrete fin-count and categorical Vt-flavor variables	Gradual improvement with elitism	Moderate
PSO [28]	Velocity-based particle swarm in continuous space	Requires rounding/ discretization of fin count and Vt, risking infeasible points	Fast initial convergence, prone to premature convergence on multimodal landscapes	Moderate-Low
DE [29]	Vector-difference mutation, primarily continuous	Needs repair operators for integer/categorical constraints	Fast on continuous benchmarks; less established for mixed-discrete circuit sizing	Moderate
ACO [30]	Pheromone-based construction over a discretized solution graph	Naturally suited to discrete fin-count/Vt choices once mapped to a graph	Can be slow for large discrete graphs; sensitive to pheromone parameters	Higher
ML/Surrogate (CNN-NSGA-II) [27]	Surrogate model trained on simulated data, guiding a multi-objective GA search	Reduces expensive SPICE evaluations once trained	Requires upfront design-of-experiments training data	Low after training, high upfront cost

This comparison indicates that GA and ACO are the most naturally suited to the present discrete design space, since fin count and threshold-voltage flavor are inherently categorical/integer variables rather than continuous ones, whereas PSO and DE require additional discretization or repair mechanisms that can bias the search. The CNN-informed NSGA-II approach of Zheng et al. [27] shows that, once a surrogate model is available, ML-assisted multi-objective GAs can further reduce the number of SPICE simulations required; extending the present GA framework with a similar surrogate model is identified as a direction for future work rather than a limitation of the present results, since the optimization reported here relies on full SPICE-level Spectre simulation for every fitness evaluation, giving greater confidence in the absolute accuracy of the reported leakage, power, and delay values at the cost of a higher simulation runtime than a surrogate-assisted approach would require.

AREA, LAYOUT, AND PRACTICAL IMPLEMENTATION ANALYSIS

Although the present study focuses primarily on electrical performance, practical SRAM design also requires area, layout, and manufacturability considerations. A first-order layout-area estimate can be derived directly from the optimized fin counts in Table 1. Using the optimized PU:AX:PD ratio of 1:2:3 and the transistor count of each topology (6, 7, 8, 9, and 10 devices respectively), and assuming a fixed per-fin layout pitch typical of 18 nm FinFET standard-cell libraries, the relative bit-cell area scales approximately with total fin count as follows: the 6T cell serves as the 1.0x reference; the 7T cell requires approximately 1.10x-1.15x the area of the 6T cell due to the extra gating device; the 8T cell requires approximately 1.30x-1.35x due to the two additional read-access transistors and the third bit-line (RBL); the 9T cell requires approximately 1.40x-1.50x; and the 10T cell requires approximately

1.60x-1.70x, consistent with its four additional read/write-access devices.

Layout complexity increases correspondingly. The 6T and 7T cells require only the standard BL/BLB and WL routing tracks, whereas the 8T-10T cells require at least one additional read bit-line (RBL) and read word-line (RWL), which must be routed in the same metal layers used for the conventional bit-lines and typically increases the number of vertical routing tracks per column by 30-50%. This directly impacts array-level bit-cell pitch and can constrain the minimum achievable row pitch in a dense memory macro, particularly for the 9T and 10T designs where both an additional read port and additional gating devices must be accommodated within the cell boundary.

From a reliability standpoint, decoupled-read topologies (8T-10T) are inherently more robust to random dopant fluctuation and fin-line-edge-roughness-induced Vt variation, because the read operation no longer disturbs the storage nodes; this is expected to translate into improved yield at the array level despite the larger cell footprint. All five topologies were sized using fin counts and threshold-voltage options that are standard offerings in mature 18 nm FinFET process design kits, so none of the optimized designs requires a non-standard device or exotic process step, and the proposed sizing is therefore expected to be manufacturable using existing 18 nm FinFET foundry flows. The main practical trade-off remains the area-versus-stability balance discussed above: designers targeting maximum array density (e.g., last-level cache) may prefer the optimized 6T or 7T cell despite its narrower noise margins, whereas designers targeting high-reliability, low-leakage memory (e.g., IoT or automotive-grade SRAM) are better served by the optimized 9T topology (highest RSNM) characterized in this work.

CONCLUSION

The performance comparison presented in Table 1 indicates that the optimized SRAM cells were re-characterized at a lower supply voltage of 1 V, compared to 1.5 V for the default designs. This voltage difference confounds a direct, like-for-like comparison of the reported values: because SNM and delay both scale with supply voltage, the changes between default and optimized rows in Table 1 cannot be attributed to transistor sizing alone, and this is acknowledged here as a limitation of the present comparison (see the Limitations section). With that caveat, the optimized leakage power and dynamic power are lower than the default values for all five topologies. Propagation delay is reduced for most topologies but not uniformly: optimized read delay for the 7T and 10T cells and optimized write delay for the 9T and 10T cells are higher, not lower, than their default values (Table 1), so the claim of a delay reduction does not hold across every cell and metric. Similarly, HSNM, RSNM, and WSNM are lower for the optimized designs than for the default designs in every topology, except 10T WSNM, which is unchanged (90 mV); the optimization therefore did not increase static noise margin, and any statement to that effect in this paper should be read as describing the intended fitness-function objective rather than an outcome confirmed by Table 1. The Genetic Algorithm-based transistor sizing approach, resulting in a PU:AX:PD ratio of 1:2:3 for every topology, is associated with the reported power reductions, but the fact that all five structurally different topologies converge to the identical discrete ratio has not been independently explained and is flagged as an open question in the Limitations section. These results indicate that the proposed optimization methodology improves leakage and dynamic power at a reduced supply voltage, with an accompanying reduction in noise margin and a mixed effect on delay that should be clarified in future iso-voltage comparisons.

In addition to the electrical performance results summarized above, the power-delay trade-off, area/layout, and qualitative benchmarking analyses presented in this paper indicate that the choice among the optimized 6T-10T topologies should be guided by application-level priorities: read-stability-critical designs benefit most from the 9T cell, whereas area-constrained designs remain best served by the optimized 6T or 7T cell.

LIMITATIONS

Several limitations of the present study should be noted explicitly. First, the default (1.5 V) and GA-optimized (1 V) cells in Table 1 were characterized at different supply voltages; because SNM and delay both scale with VDD, the reported differences cannot be attributed to transistor sizing alone; an iso-voltage comparison

(both designs at either 1.5 V or 1 V) is needed before the optimization's effect on SNM and delay can be isolated from the voltage effect. Second, the optimized HSNM, RSNM, and WSNM in Table 1 are lower than the corresponding default values for every topology except 10T WSNM (unchanged); the stated goal of maximizing SNM was not achieved by the reported results, and the optimization should instead be described as improving leakage and dynamic power at the cost of noise margin and (for some topologies and metrics) at the cost of delay. Third, the Genetic Algorithm is reported to converge to the identical PU:AX:PD ratio of 1:2:3 for all five structurally different topologies; this outcome is not independently explained in the manuscript and, combined with the unverified reproducibility statistics discussed in the GA Parameter Settings, Convergence, and Repeatability section, means the GA results should be treated as provisional pending confirmation against actual simulation logs. Fourth, Figs. 8–10 are screen captures of the simulator butterfly curves; the extracted SNM values are listed in Table 1.

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